Al(Cu) layer 93 and metal layers 92-94 are patterned by RIE. TiN layer 94 is provided on the Al(Cu) layer 93 to reduce reflections so that fine features can be patterned by photolithography. Titanium nitride was used on the surface of reflector/absorber layer 34 since the necessary process steps were already available even though a lower red reflectivity would be desirable. One possibility would be to add carbon to the TiN: TiN0.33 C0.67 has been reported in "Optical Constants and Spectral Selectivity of Titanium Carbonitrides", by B. Karlsson, Thin Solid Films, p. 181, 87 (1982) to have a reflectivity of about 30% for all the wavelengths of interest. After the reflector/absorber layer 34 is patterned, a 400-500 nm layer of Si3 N4 is deposited to form dielectric layer 46 as shown in FIG. 7. The thickness of dielectric layer 46 is a compromise between a thinner layer for greater capacitance between reflector/absorber layer 34 and electrode/mirror 30 and a thicker layer which would reduce the probability of reflector/absorber layer 34 and electrode/mirror 30 defects and shorts.

Amend the paragraph bridging pages 21 and 22 as follows:

Starting from the Si devices 100, a total of eight masks would be needed (three metal levels M1(102), M2(104) and M3(106), three via/stud levels 50(112), 52(114) and 53(116), and two insulator levels). Starting at the S1 level 114, FIG. 12, the [reflector/absorber] M2 layer [34] 104, which is preferably formed of TiN/Al(Cu)/Ti, is patterned to function as the reflector/absorber layer 34 within spatial light modulator array 10 and as M2 wiring outside of the array area of spatial light modulators 10 as shown in FIG. 13. The planarized SiO2 120 over electrode/mirror 30 is capped with an Si3 N4 dielectric layer 46 which is used as an etch stop between mirrors during the etching of dielectric layer 32 to form spacer posts 32 as shown in FIG. 17. Inside the spatial light modulator array 10, to get the most effective light shielding, the S2 116 stud is stacked directly on the S1 114 stud as shown in FIG. 15. Alternatively, an M2 104 segment could be interposed between the two studs but this would require a larger break in the M2/AR layer 104 which would be more likely to permit light through to the semiconductor substrate below. The M3 mirror layer 106 is formed by Al or Al(Cu)